

USSN 10/068,159

PATENT RESPONSE

AMENDED CLAIMS

1. (previously amended) A stacked die assembly, comprising:

at least two semiconductor dies disposed on a substrate in a stacked arrangement; the substrate comprising a first surface having terminal pads disposed thereon, and a second surface; a first die disposed on the first surface of the substrate, and comprising a first surface having bond pads disposed thereon, a second surface, and bonding elements connecting the bond pads to the terminal pads on the substrate; and

a second die comprising a first surface, a second surface, and a perimeter; the first surface having bond pads disposed thereon; the second surface comprising a recessed edge portion along the perimeter of the die; the second die disposed on the first surface of the first die with the bond pads on the first die positioned within the recessed edge portion; the recessed edge portion having a height sufficient for clearance of the bonding elements extending from the bond pads of the first die.

2. (previously amended) A stacked die assembly, comprising:

at least two semiconductor dies disposed on a substrate in a stacked arrangement; the substrate comprising a first surface having terminal pads disposed thereon, and a second surface;

a first die disposed on the first surface of the substrate; the first die comprising an active surface having bond pads disposed thereon, an opposing inactive surface, and bonding elements connecting the bond pads of the first die to the terminal pads on the substrate; and

a second die comprising an active surface, an opposing inactive surface, and a perimeter; the active surface having bond pads disposed thereon; the inactive surface having a recessed edge portion along the perimeter of the die; the second die disposed on the active surface of the first die with the recessed edge portion providing an opening over the bond pads of the first die, the opening sufficient for passage of the bonding elements therethrough.

USSN 10/068,159

PATENT RESPONSE

3. (previously amended) A stacked die assembly, comprising:

at least two semiconductor dies disposed on a substrate in a stacked arrangement; the substrate comprising a surface having terminal pads disposed thereon;

a first die disposed on said surface of the substrate; the first die comprising a first surface having bond pads disposed thereon, a second surface, and bonding elements connecting the bond pads of the first die to the terminal pads on the substrate; and

a second die comprising a first surface, an opposing second surface, and a perimeter; the first surface having bond pads disposed thereon; the second surface having a thickness removed along the perimeter of the die to provide a recessed edge portion; the second die disposed on the first surface of the first die with the bond pads of the first die disposed within the recessed edge portion; the recessed edge portion having a sufficient height for clearance of the bonding elements extending from the bond pads on the first die.

4. (previously amended) A stacked die assembly, comprising:

at least two semiconductor dies disposed on a substrate in a stacked arrangement; the substrate comprising a surface having terminal pads disposed thereon;

a first die disposed on said surface of the substrate; the first die comprising a first side having bond pads disposed thereon, an opposing second side, and bonding elements connecting the bond pads of the first die to the terminal pads on the substrate; and

a second die comprising a first side, an opposing second side, and a perimeter; the first side having bond pads disposed thereon; the second side comprising a recessed edge portion along the perimeter of the die; the second die disposed on the first side of the first die with the bond pads of the first die disposed within the recessed edge portion of the second die, the recessed edge portion having a height sufficient for passage of the bonding elements from the bond pads of the first die therethrough.

5. (previously amended) The die assembly of Claim 4, further comprising: bonding elements connecting the bond pads of the second die to the terminal pads on the substrate.

862130v1

USSN 10/068,159

PATENT RESPONSE

6. (original) The die assembly of Claim 4, further comprising: at least one of an adhesive element disposed between the first die and the substrate, and an adhesive element disposed between the second die and the first die.

7. (original) The die assembly of Claim 6, wherein the adhesive element comprises a die attach adhesive.

8. (original) The die assembly of Claim 6, wherein the adhesive element comprises a tape adhesive.

9. (original) The die assembly of Claim 4, wherein the second die has at least one of a length and a width greater than the first die.

10. (original) The die assembly of Claim 4, wherein the bonding element comprises a TAB tape.

11. (original) The die assembly of Claim 4, wherein the bonding element comprises a wire bond.

12. (original) The die assembly of Claim 4, wherein the substrate comprises a material selected from the group consisting of bismaleimide triazine resin, epoxy resins, ceramics, and polyimide resins.

13. (original) The die assembly of Claim 4, wherein the substrate comprises a metal leadframe.

14. (original) The die assembly of Claim 4, being at least partially encapsulated.

15 - 23. (cancelled)

862130v1

USSN 10/068,159

PATENT RESPONSE

15

74. (previously amended) A stacked die assembly, comprising:

a plurality of semiconductor dies disposed on a substrate in a stacked arrangement; the substrate comprising a first surface having terminal pads disposed thereon, and a second surface;

a first die disposed on the first surface of the substrate, and comprising a first surface and a second surface having a recess formed therein; and

a second die at least partially disposed in the recess of the first die, and comprising a first surface having bond pads disposed thereon, an opposing second surface disposed on the first die, and bonding elements connecting the bond pads of the second die to the terminal pads on the substrate; and

a third die comprising a first surface, an opposing second surface, and a perimeter; the first surface having bond pads disposed thereon; and the second surface comprising a recessed edge portion along the perimeter; the second surface of the third die disposed on the first surface of the second die whereby the recessed edge portion provides sufficient clearance for the bonding elements extending from the bond pads of the second die.

16

75. (previously amended) A stacked die assembly, comprising:

a plurality of semiconductor dies disposed on a substrate in a stacked arrangement; the substrate comprising a first surface having terminal pads disposed thereon, and a second surface;

a first die comprising a first surface disposed on the first surface of the substrate in a flip chip attachment, and a second surface having a recess, the recess having a surface; and

a second die at least partially disposed in the recess of the first die, and comprising a first surface having bond pads disposed thereon, an opposing second surface disposed on the surface of the recess, and bonding elements connecting the bond pads of the second die to the terminal pads on the substrate; and

a third die comprising a first surface, an opposing second surface, and a perimeter; the first surface having bond pads disposed thereon; and the second surface comprising a recessed edge portion along the perimeter; the second surface disposed on the first surface of the second die whereby the recessed edge portion provides sufficient clearance for the bonding elements extending from the bond pads of the second die.

862130v1

USSN 10/068,159

PATENT RESPONSE

¹⁷
~~26~~. (original) The die assembly of Claim ^{1b}~~25~~, wherein the recess in the first die is substantially square or rectangular shaped.

¹⁸
~~27~~. (original) The die assembly of Claim ^{1b}~~25~~, wherein the recess in the first die is substantially oval or circular shaped.

¹⁹
~~28~~. (previously amended) The die assembly of Claim ^{1b}~~25~~, further comprising: bonding elements connecting the bond pads of the third die to the terminal pads on the substrate.

²⁰
~~29~~. (original) The die assembly of Claim ^{1b}~~25~~, further comprising: at least one of an adhesive element disposed between the first die and the second die, and an adhesive element disposed between the second die and the third die.

²¹
~~30~~. (original) The die assembly of Claim ^{1b}~~25~~, wherein the third die has at least one of a length and a width greater than the second die.

²²
~~31~~. (original) The die assembly of Claim ^{1b}~~25~~, being at least partially encapsulated.

²³
[~~32~~. (cancelled)

USSN 10/068,159

PATENT RESPONSE

23

33. (previously amended) A stacked die assembly, comprising:

at least two semiconductor dies disposed on a substrate in a stacked arrangement; the substrate comprising a first surface having terminal pads disposed thereon, and a second surface;

a first die disposed on the first surface of the substrate; the first die comprising a first surface having bond pads disposed thereon, and an opposing second surface having a recess formed therein; the first die attached to the substrate by an adhesive element disposed within the recess; and bonding elements connecting the bond pads of the first die to the terminal pads on the substrate; and

a second die comprising a first surface, an opposing second surface, and a perimeter; the first surface having bond pads disposed thereon; the second surface comprising a recessed edge along the perimeter; and the second die disposed on the first surface of the first die whereby the recessed edge provides sufficient clearance for the bonding elements extending from the first die.

24

23

34. (original) The die assembly of Claim 33, wherein the adhesive element disposed within the recess comprises one of a die attach adhesive, and a tape adhesive.

25

23

35. (original) The die assembly of Claim 33, further comprising: a second adhesive element disposed between the first die and the second die.

26

23

36. (previously amended) The die assembly of Claim 35, further comprising: bonding elements connecting the bond pads of the second die to the terminal pads on the substrate.

27

23

37. (original) The die assembly of Claim 33, wherein the second die has at least one of a length and a width greater than the first die.

28

23

38. (original) The die assembly of Claim 33, being at least partially encapsulated.

39 - 46. (cancelled)

USSN 10/068,159

PATENT RESPONSE

²⁹
47. (previously amended) A semiconductor die package, comprising the die assembly of Claim 1, further comprising bonding elements connecting the bond pads of the second die to the terminal pads on the substrate, and being at least partially encapsulated.

³⁰ ²⁹
48. (previously amended) The package of Claim 47, further comprising: external contacts disposed on the second surface of the substrate.

³¹ ³⁰
49. (original) The package of Claim 48, wherein the external contacts comprise a conductive solder, conductive epoxy, or conductor-filled epoxy.

³² ³⁰
50. (original) The package of Claim 48, wherein the external contacts are in the form of balls, columns, pins, or a combination thereof.

51. (cancelled)

³³
¹⁵ 52. (previously amended) A semiconductor die package, comprising the die assembly of Claim 24, further comprising bonding elements connecting the bond pads of the third die to the terminal pads on the substrate, and being at least partially encapsulated.

53 - 111. (cancelled)

USSN 10/068,159

PATENT RESPONSE

34

112. (previously amended) A stacked die assembly, comprising:

at least two semiconductor dies disposed on a substrate in a stacked arrangement; the substrate comprising a first surface having terminal pads disposed thereon, and a second surface;

a first die disposed on the first surface of the substrate, and comprising a first surface having bond pads disposed thereon, a second surface, and bonding elements connecting the bond pads to the terminal pads on the substrate; and

a second die comprising a first surface, a second surface, and a perimeter; the first surface having bond pads disposed thereon; the second surface comprising a recessed edge portion along the perimeter of the die; the second die disposed on the first surface of the first die with the bond pads on the first die positioned within the recessed edge portion; the recessed edge portion having a height sufficient for clearance of the bonding elements extending from the bond pads of the first die;

means for mounting the first die on the substrate;

means for mounting the second die on the first die; and

means for connecting the bond pads of the first die to the terminal pads on the substrate.

35

34

113. (previously added) The assembly of Claim 112, wherein the mounting means comprises a die-attach adhesive, a tape adhesive, or a combination thereof.

36

34

114. (previously added) The assembly of Claim 112, wherein the connecting means comprises a wire bond.

37

34

115. (previously added) The assembly of Claim 112, wherein the connecting means comprises a TAB tape.

38

34

116. (previously added) The assembly of Claim 112, further comprising means for connecting the assembly to an external electrical apparatus.

39

38

117. (previously added) The assembly of Claim 116, wherein the assembly connecting means comprises a conductive solder, conductive epoxy, or conductor-filled epoxy, attached to the second surface of the substrate.

USSN 10/068,159

PATENT RESPONSE

40 38
118. (previously added) The assembly of Claim 116, wherein the assembly connecting means are in the form of balls, columns, pins, or a combination thereof, attached to the second surface of the substrate.

41 34
119. (previously added) The assembly of Claim 112, being at least partially encapsulated to form a die package.

120 - 123. (cancelled)

42
124. (previously added) A stacked die assembly, comprising:
a plurality of semiconductor dies disposed on a substrate in a stacked arrangement; the substrate comprising a first surface having terminal pads disposed thereon, and a second surface;
a first die disposed on the first surface of the substrate, and comprising a first surface and a second surface having a recess formed therein; and
a second die at least partially disposed in the recess of the first die, and comprising a first surface having bond pads disposed thereon, an opposing second surface disposed on the first die; and
a third die comprising a first surface, an opposing second surface, and a perimeter; the first surface having bond pads disposed thereon; and the second surface comprising a recessed edge portion along the perimeter, the second surface of the third die disposed on the first surface of the second die;

means for mounting the first die on the substrate;
means for mounting the second die in the recess of the first die;
means for mounting the third die on the second die; and
means for connecting the bond pads of the second and third dies to the terminal pads on the substrate.

whereby the recessed edge portion of the third die provides sufficient clearance for the connecting means extending from the bond pads of the second die to the substrate.

43 42
125. (previously added) The assembly of Claim 124, wherein the mounting means of the first die comprises a flip chip attachment.

USSN 10/068,159

PATENT RESPONSE

44

136. (previously added) The assembly of Claim 124, further comprising means for connecting the assembly to an external electrical apparatus.

42

45

137. (previously added) The assembly of Claim 124, being at least partially encapsulated to form a die package.

128 - 136. (cancelled)

46

137. (previously added) An apparatus, comprising:
an electrical apparatus; and

the die package of Claim 119 in electrical communication with the electrical apparatus.

47

46

138. (previously added) The apparatus of Claim 137, wherein the electrical apparatus is selected from the group consisting of a PCB, motherboard, program logic controller, and testing apparatus.

48

139. (previously added) An apparatus, comprising:
an electrical apparatus; and

41

the die package of Claim 119 in electrical communication with the electrical apparatus.

140. (cancelled)

49

141. (previously added) An apparatus, comprising:
an electrical apparatus; and

45

the die package of Claim 121 in electrical communication with the electrical apparatus.

142 - 143. (cancelled)

50

144. (previously added) A panel substrate, comprising multiple die assemblies according to Claim 1.

C

USSN 10/068,159

PATENT RESPONSE

145. (cancelled)

51
146. (previously added) A panel substrate, comprising multiple die assemblies according to Claim 24.15

147 - 148. (cancelled)

52
149. (previously added) A stacked die assembly, comprising:
at least two semiconductor dies disposed on a substrate in a stacked arrangement; the substrate comprising a first surface having terminal pads disposed thereon, and a second surface;
a first die disposed on the first surface of the substrate, and comprising first and second surfaces, bond pads disposed on the first surface, and bonding elements interconnecting the bond pads and the terminal pads; and
a second die disposed on the first surface of the first die, and comprising first and second surfaces, a perimeter, bond pads disposed on the first surface, and the second surface comprising a recessed edge portion along the perimeter of the die; the bond pads on the first die positioned within the recessed edge portion; the recessed edge portion having a height sufficient for clearance of the bonding elements interconnecting the bond pads of the first die and the terminal pads on the substrate.

53
150. (previously added) A stacked die assembly, comprising:
a first die disposed on a substrate, a second die disposed on the first die in a stacked arrangement, and bonding elements interconnecting bond pads disposed on the first die to terminal pads disposed on the substrate, the bonding elements disposed within a recessed edge portion along a perimeter of the second die, the recessed edge portion having a height sufficient for clearance of the bonding elements.

54
151. (previously added) The die assembly of Claim 150, further comprising: bonding elements connecting bond pads disposed on the second die to terminal pads on the substrate.

53

USSN 10/068,159

PATENT RESPONSE

⁵⁵
152. (previously added) The die assembly of Claim ⁵³150, further comprising: an adhesive element disposed on a surface of the first die between the substrate, the second die, or both.

⁵⁶
153. (previously added) The die assembly of Claim ⁵³150, wherein the second die has at least one of a length or a width greater than the first die.

⁵⁷
154. (previously added) The die assembly of Claim ⁵³150, wherein the substrate comprises a leadframe.

⁵⁸
155. (previously added) The die assembly of Claim ⁵³150, being at least partially encapsulated.

⁵⁹
156. (previously added) The die assembly of Claim ⁵³150, wherein the first die is attached to the substrate by an adhesive element disposed within a recess within a surface of the die.

⁶⁰
157. (previously added) The die assembly of Claim ⁵³150, wherein the first die comprises first and second surfaces, the second die being disposed on the second surface, and the first surface comprising a recess.

⁶¹
158. (previously added) The die assembly of Claim ⁶⁰157, wherein an adhesive element is disposed within the recess of the first die.

⁶²
159. (previously added) The die assembly of Claim ⁶⁰157, wherein a third die is disposed within the recess of the first die.

⁶³
160. (previously added) A panel substrate, comprising multiple die assemblies according to Claim ⁵³150.

⁶⁴
161. (previously added) An apparatus, comprising:

an electrical apparatus; and

the die assembly of Claim 150 in electrical communication with the electrical apparatus.